[APPLICATION] Technique for implementing a security algorithm
US Pat. 10730203 - Filed Dec 4, 2003
In **pipeline stage** 2310, the result of **stage** 1 is added to the chaining **...** if an operation performed in **iteration** 2 of the **inner loop** is dependent upon data **...**

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In **pipeline stage** 2310, the result of **stage** 1 is added to the chaining **...** [0031] Because the **inner loop** is executed 80 times in order to process 512 bits, **...**

Method and apparatus for prefetching recursive data structures
US Pat. 6848029 - Filed Jan 3, 2001
5, 6, 10, and 11 and is described for search tree traversals and **hash** tables below. **...** a single pass of the **inner loop** of the search below does not require **...**

Outer join operations using responsibility regions assigned to **inner** tables ...
US Pat. 5557791 - Filed Oct 19, 1994 - International Business Machines Corporation
At a given scan position, if no tuple of the **inner** table matches the 60 outer **...** nested **loop**, merge join, hybrid join, and **hash** join) with minimal extra **...**

Program storage device and computer program product for outer join ...
US Pat. 5551031 - Filed Jun 7, 1995 - International Business Machines Corporation
At a given scan position, if no tuple of the **inner** table matches the 60 outer **...** nested **loop**, merge join, hybrid join, and **hash** join) with minimal extra **...**

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System and process for application-**level** flow connection of data processing ...
US Pat. 6226267 - Filed Apr 10, 1998 - Top Layer Networks, Inc.
The results of the **parallel** hashing are placed in **Hash** FIFO 393 and compared **...**
With the flow parameters determined, an appropriate **instruction** is issued **...**

System and process for GHIH-speed pattern matching for application-**level** ...
US Pat. 6430184 - Filed Apr 10, 1998 - Top Layer Networks, Inc.
The results of the **parallel** hashing are placed in **Hash** FIFO 393 and compared **...**
With the flow parameters determined, an appropriate **instruction** is issued **...**

Application-**level** data communication switching system and process for ...
US Pat. 6426943 - Filed Apr 3, 1999 - Top Layer Networks, Inc.
The results of the **parallel** hashing are placed in **Hash** FIFO 393 and **...** With the flow parameters 25 determined, an appropriate **instruction** is issued by CPU **...**

Processor assigning data to hardware partition based on selectable **hash** of ...
US Pat. 6470442 - Filed Jul 30, 1999 - International Business Machines Corporation
In within the subset defined by a **hash** are stored in rename and addition, **...** of rename and architected registers allocated **parallel** to each **hash** may be **...**

Bulk-synchronous **parallel** computer
US Pat. 5083265 - Filed Apr 17, 1990 - President and Fellows of Harvard College
Hash functions for this **parallel** context have been high performance **hash** functions, Proc. 30th IEEE proposed and analyzed in K. Mehlhorn and U. Vishkin, **...**

Microprocessor and data flow microprocessor having vector operation function
US Pat. 5666535 - Filed Oct 28, 1994 - Mitsubishi Denki Kabushiki Kaisha
However, in the event of memory address of 24 bits, and the packet having an **hash** conflict, it is necessary to access the memory sequen- **instruction** code of **...**

Microprocessor and data flow microprocessor having vector operation function
US Pat. 5404553 - Filed Jan 2, 1992 - Mitsubishi Denki Kabushiki Kaisha
... packet having an **instruction** code of memory access is MM, the **parallel hash** method **...** it 30 (8) Memory space of practical **level** may be compared to the **...**

Atomic network switch with integrated circuit switch nodes
US Pat. 5802054 - Filed Aug 16, 1996 - 3Com Corporation
Typically a 500 in **parallel** to **hash** flow logic 1 through **hash** flow logic router **...** after a special **instruction** is defined by a vector register specifying **...**

Atomic network switch with integrated circuit switch nodes

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Dynamic configurable system of **parallel** modules comprising chain of chips ...
US Pat. 6112288 - Filed May 19, 1998 - Paracel, Inc.
The **instruction** processor's internal registers may be configured as a **shift register** for initialization or diagnostics. In this mode, instructions exit the **...**

Parallel searching for an **instruction** at multiple cache levels
US Pat. 6848031 - Filed Jan 2, 2002 - Intel Corporation
For example, the **shift register** 56 and/or gate 58 can be incorporated with **...** at a second **level** for the **instruction** in **parallel** with the first **level** based **...**

Superscalar processor with plural pipelined execution units each unit ...
US Pat. 5530804 - Filed May 16, 1994 - Motorola, Inc.
When the 5-bit value is loaded, apply pin 46 will be asserted to load serial **shift register** 48 contents into the 25 **parallel** command register 50. 3. **...**

Adaptive **instruction** processing by array processor having processor ...
US Pat. 4783738 - Filed Mar 13, 1986 - International Business Machines Corporation
1-7, shows details of operation of program control unit includes a flag register which NCR's geometric arithmetic **parallel** helps keep the **instruction** size **...**

Multi-layer switching apparatus and method
US Pat. 6424659 - Filed Jul 17, 1998 - Network Equipment Technologies, Inc.
The multi-**level** packet switching system of claim 5 wherein the **hash** look-up **...** of pipeline buffers coupled to said Reduced **Instruction** Set Computer (RISC) **...**

Error tolerant microprocessor
US Pat. 4866718 - Filed Aug 25, 1987 - Galaxy Microsystems, Inc.
and on the degree of paralleling or **pipelining** of operations implemented. **...** each stage of said **parallel shift register** storing a multi- bit error code **...**

Control of **instruction** pipeline in data processing system
US Pat. 4365311 - Filed Aug 31, 1978 - Hitachi, Ltd.
... of the timing in **parallel** execu- steps allotted to said each segment, **...** supplying means comprises a **shift register** having { programmed instructions, **...**

System for restoring **register** data in a pipelined data processing system ...
US Pat. 6065107 - Filed Aug 28, 1998 - International Business Machines Corporation
One popular technique to increase pro- 20 cessing speed is "**pipelining**", **...** VLIW fine-grained parallelism exists at the machine **instruction level** within **...**

System for restoring **register** data in a pipelined data processing system ...
US Pat. 5875348 - Filed Sep 13, 1996 - International Business Machines Corporation

Google patents minimize critical path pipelining hash OR "shift Search Patents Advanced

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Multi-channel analogue to digital convertor
US Pat. 5099239 - Filed Sep 21, 1989 - Xerox Corporation
Second, the layout has 15 tion from the ADC 16 to the **shift register** 20 and the a **...** several features **minimize** this control **path** 30 thus minimizing the **...**

Method and apparatus for operating a data processor to execute software ...
US Pat. 6044220 - Filed Feb 25, 1997 - Motorola, Inc.
8 illustrates in tabular form a **hash** table implementation **....** a constant stream of instructions to CPU 201 in order to **minimize** pipeline stalls and to make **...**

Analog to digital converter utilizing a semiconductor capicitor array
US Pat. 5140327 - Filed Apr 1, 1991 - Xerox Corporation
Pipelining is illustrated in cycles 2 and 3. A second analog signal is integrated **... shift register** while CS1 is charged to the second input voltage level. **...**

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[0005] In general, **hash** algorithms are algorithms that take a large group **...** as to **minimize** the **critical path** associated with long dependency chains among **...**

Interface for connecting a bus to a random access memory using a two wire ...
US Pat. 5724537 - Filed Mar 6, 1997 - Discovision Associates
12 Verification control **shift-register** must now produce control signals of **...** the results of the **Critical Path** Analysis (CPA) configuration problems. **...**

Interface for connecting a bus to a random access memory using a swing ...
US Pat. 5956741 - Filed Oct 15, 1997 - Discovision Associates
It is important to **minimize** the number of "overs" latch, (vertical wires not **...** results of the **Critical Path** Analysis (CPA) 65 adequately at that level. **...**

Code converter for data compression/decompression
US Pat. 4853696 - Filed Apr 13, 1987 - University of Central Florida
It should be noted that the **critical** delay which determines the clock speed is the delay within the decoder 72. To **minimize** this delay, the decoder 72 can **...**

[APPLICATION] Multistandard video decoder and decompression system for processing encoded ...
US Pat. 9776641 - Filed Feb 5, 2001
1.3 Transform Datapath and Control **Shift- Register** [2712] It is possible to **...** also used to verify the results of the **Critical Path** Analysis (CPA) tool in **...**

Branch predictor using random access memory
US Pat. 4370711 - Filed Oct 21, 1980 - Control Data Corporation